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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,987	10/22/2003	Yoshikazu Kasuya	117575	8987
25944	7590	06/16/2005		
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER LUU, CHUONG A	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/689,987

Applicant(s)

KASUYA, YOSHIKAZU

Examiner

Chuong A. Luu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 8-12 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/24/2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION*****Election/Restrictions***

Applicant's election with traverse of method Group I, claims 1-7, which filed on February 24, 2005 is acknowledged. The traversal is on the ground(s) that a search and examination of the entire application would not place a serious burden on the Examiner. This is not found persuasive, because group I, claims 1-7, drawn to a semiconductor device, classified in class 257, subclass 316 and group II, claims 8-12 drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 266 are drawn to distinct inventions as noted in the previous office action. Applicant's objection to the restriction requirement is noted but the fact that the two groups fall in two different classes would require two different searches and is therefore an undue burden.

The requirement is still deemed proper and is therefore made FINAL.

**PRIOR ART REJECTIONS****Statutory Basis****Obvious Type Double Patenting**

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double

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patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 17-33 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 of Inoue (U.S. Application No. 10/635,562). Inoue teaches the basic features of applicant's claims but does not specifically claim the upper most layer of the second insulating layer is a charge transfer protection film. However, the manner of applying upper most layer of the second insulating layer is a charge transfer protection film is taught in Inoue. Therefore, it would have been obvious to one of ordinary skill in the art to recognize the teaching of Inoue by applying the upper most layer of the second insulating layer is a charge transfer protection film to exceed its performance criteria. For these reasons, claim 1-7 are seen as obvious variations of the patented claims.

## **PRIOR ART REJECTIONS**

### **Statutory Basis**

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

### **The Rejections**

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Ebina et al. (U.S. 6,518,124 B1).

Ebina discloses a semiconductor device with

(1) a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,

wherein each of the non-volatile memory devices has:

a word gate formed above a semiconductor layer with a gate insulating layer interposed;

an impurity layer formed in the semiconductor layer to form a source region or a drain region;

control gates in the form of side walls formed along both side surfaces of the word gate;

wherein each of the control gate consists of a first control gate and a second control gate adjacent to each other;

wherein a first insulating layer is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;

wherein a second insulating layer is disposed between the second control gate and the semiconductor layer;

wherein the thickness of the second insulating layer is less than the thickness of the first insulating layer;

wherein an upper most layer of the second insulating layer is a charge transfer protection film (see Figure 3);

(2) wherein the first insulating layer is a stack of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film (see Figure 3);

(3) wherein the second insulating layer is a stack of a silicon oxide film, a silicon nitride film and the charge transfer protection film, the thickness of the charge transfer protection film being less than the thickness of the second silicon oxide film of the first insulating layer (see Figure 3);

(4) wherein the charge transfer protection film is further provide on a surface of the first control gate (see Figure 3);

(5) wherein the charge transfer protection film is one of a silicon oxide film and a silicon oxide nitride film (see Figure 3);

(6) wherein the charge transfer protection film is further provide on a surface of the first control gate (see Figure 3);

(7) wherein the charge transfer protection film is further provide on a surface of the first control gate (see Figure 3).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Chuong Anh Luu  
Patent Examiner  
June 10, 2005